	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
1	BRS	L1	1	wu near kuo-chien.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 11:11	
2	BRS	L2	19	chen near yi-nan.in.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 11:12	
3	BRS	L3	1531	438/257.ccls.	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 12:07	
4	BRS	L4	196	(remov$3) near5 (conduct$3) near15 (bit near line)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:27	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
5	BRS	L5	298	(remov$3) near5 (conduct$3) near15 (bit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:57	
6	BRS	L6	0	(remov$3) near5 (stop near layer) near15 (bit) near25 (barrier near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:58	
7	BRS	L7	16	(remov$3) near5 (stop near layer) near15 (bit)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:57	
8	BRS	L8	2	(stop near layer) near15 (bit) near25 (barrier near layer)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 15:59	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
9	BRS	L9	4	(stop near layer) near15 (bit) near25 (remov$3 near15 conduct$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:05	
10	BRS	L10	8	(barrier near layer) near15 (bit) near25 (remov$3 near15 conduct$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:14	
11	BRS	L11	2109	(memory) near15 (peripheral or driver) near25 (bit near line)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:15	
12	BRS	L12	30	(memory) near15 (peripheral or driver) near25 (bit near line) near20 (conduct$3) near15 (dielectric or insulat$3)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:33	

	Type	L #	Hits	Search Text	DBs	Time Stamp	Comments
13	BRS	L13	33	(peripheral or driver) near25 (bit near line) near20 (conduct$3) near15 (dielectric or insulat$3)near30 (contact)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:43	
14	BRS	L14	2898	(bit near line near contact$1) near15 (bit near line)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:45	
15	BRS	L15	113	(bit near line near contact$1) near15 (bit near line) near15 (memory near device)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:51	
16	BRS	L16	147	(bit near line near15 equal) near15 (bit near line) near15 (memory near device)	USPAT; US-PGPUB; EPO; JPO; DERWENT; IBM_TDB	2004/02/09 16:51	

	U	1	Document ID	Title	Current OR	Pages	Issue Date
1	☒	☐	US 20030214022 A1	Bit line landing pad and borderless contact on bit line stud with localized etch stop layer formed in void region, and manufacturing method thereof	257/678	11	20031120
2	☒	☐	US 20030186530 A1	Methods of fabricating buried digit lines	438/622	18	20031002
3	☒	☐	US 20020195635 A1	Methods of fabricating buried digit lines and semiconductor devices including same	257/296	18	20021226
4	☒	☐	US 20020068440 A1	Methods of fabricating buried digit lines and semiconductor devices including same	438/637	18	20020606
5	☐	☐	US 6555463 B2	Methods of fabricating buried digit lines	438/622	17	20030429
6	☐	☐	US 6475857 B1	Method of making a scalable two transistor memory device	438/240	20	20021105
7	☐	☐	US 6452223 B1	Methods of fabricating buried digit lines and semiconductor devices including same	257/296	19	20020917
8	☐	☐	US 6372629 B1	Methods of fabricating buried digit lines and semiconductor devices including same	438/622	17	20020416
9	☐	☐	US 6350649 B1	Bit line landing pad and borderless contact on bit line stud with etch stop layer and manufacturing method thereof	438/256	11	20020226
10	☐	☐	US 6191459 B1	Electrically programmable memory cell array, using charge carrier traps and insulation trenches	257/390	12	20010220
11	☐	☐	US 6184082 B1	Method of fabricating dynamic random access memory	438/253	18	20010206

	U	1	Document ID	Title	Current OR	Pages	Issue Date
12	☒	☐	US 6180508 B1	Methods of fabricating buried digit lines and semiconductor devices including same	438/622	18	20010130
13	☒	☐	US 6010931 A	Planarization technique for DRAM cell capacitor electrode	438/240	13	20000104
14	☒	☐	US 5670404 A	Method for making self-aligned bit line contacts on a DRAM circuit having a planarized insulating layer	438/239	10	19970923
15	☒	☐	US 6020236 A	Fabrication of capacitance node contacts between underlying polysilicon bit lines in DRAM cell by using an etch stop layer to remove exposed/misaligned polysilicon bit line material, forms nitride isolation on remaining section of bit line		9	20000201
16	☒	☐	US 5670404 A	Self aligned bit line contacts on dynamic random access memory circuit - having a planarised insulating layer by using an undoped poly:silicon layer as an etch stop layer		10	19970923